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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,340	01/04/2005	Jose Solo de Zaldivar	CH02 0023 US	2662

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER

GRAHAM, KRETILIA

ART UNIT	PAPER NUMBER
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2827

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/520,340	Applicant(s) SOLO DE ZALDIVAR ET AL.	
	Examiner Kretelia Graham	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 9-13 is/are pending in the application.
- 4a) Of the above claim(s) 10-13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 10-13 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 January 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 1/23/07, with respect to the objections to the claims, drawings, and specification have been fully considered and are persuasive. The objections have been withdrawn.

2. Applicant's arguments, filed 1/23/07, with respect to the rejection(s) of claim(s) 1 under 35 USC 102 (b) in view of the US patents to Sharpe and Lin have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly discovered prior art.

Arguments regarding newly added claims 10-13 are not being addressed since the new claims are restrictable by original presentation (see below).

3. Applicant's arguments filed 1/23/07 have been fully considered but they are not persuasive.

In response to applicant's argument that the feature disclosed at **page 3, lines 15-17** of the specification is not prior art and is not inherently present in every CMOS cell, the Examiner notes that the feature of n-well diffusion region being the control gate of the floating capacitor being "inherently available in any CMOS process" (see page 3, lines 15-17) is evidence that is may be incorporated into any CMOS process with

Art Unit: 2827

success. The fact that the feature is not present in the first embodiment of the present invention and is present in the second embodiment, further supports the fact that a cell not including this feature (such as in the case of the teachings of Lin and Sharpe and the first embodiment of the invention) can be modified by one skilled in the art with success, to achieve the invention illustrated in FIG. 6-8 of the present invention.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the knowledge is generally available to one of ordinary skill in the art.

Election/Restrictions

4. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Art Unit: 2827

Group I, claim(s) 1-4 and 9, are drawn to an erasable and programmable non-volatile cell including circuitry for detecting the state of the cell whether erased or programmed.

Group II, claim(s) 10-13, are drawn to an erasable and programmable non-volatile cell comprising an n-channel transistor adaptable for programming data into the cell by having programming voltages applied to its gate, source, and drain, and a p-channel transistor adapted to read data from the cell by having appropriate read voltage applied to its gate, source, and drain.

5. The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the circuitry of Group I related to detecting the state of the cell and the circuitry of Group II relates to programming and reading the cell using respective programming and read voltages.

6. Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not

Art Unit: 2827

distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103 (a) of the other invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

8. Newly submitted claims 10-13 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: see explanation above in paragraphs 4 and 5.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 10-13 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by the US patent to Killat (6,704,221 B2), hereafter "Killat".

Pertaining to claim 1, **FIG. 3** is directed towards: an erasable and programmable non-volatile cell **210**, comprising: a first transistor **214** having a source, a drain, and gate; a floating capacitor **226** having a floating gate **218** and a control gate **230**, said floating gate being connected to said gate of said first transistor; and circuitry **222** for detecting the state, whether erased or programmed, of the cell **Note: The charge state (i.e. erased or programmed) of the cell is detected by PMOS transistor 222 (see column 4, lines 50-52)**, wherein said circuitry for detecting the state of the cell comprises a second transistor **222** having a source, a drain, and a gate, said second transistor being complementary to said first transistor and said gate of said second transistor being connected to said floating gate; and wherein the drain of the first transistor and the drain of the second transistor are electrically separated from each other such that drain currents of the first and second transistors can be determined

Art Unit: 2827

separately from each other **Note: See FIG. 3 where the drain of PMOS transistor 222 is connected output node 258 (see column 3, lines 52-54) and the drain of NMOS transistor is tied to ground potential 254, allowing for separate drain current determination (also see column 4, lines 37-52).**

Pertaining to claim 2, **FIG. 3** is directed towards: wherein said first transistor is an n-channel transistor **214** and said second transistor is a p-channel transistor **222**.

Pertaining to claim 3, **FIG. 3** is directed towards: wherein said first and second transistors are MOSFET transistors.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killat in view of the Applicant's admitted prior art.

Pertaining to claim 4; **FIG. 3** discloses: an erasable and programmable non-volatile cell **210**, comprising: a n-channel transistor **214** having a source, a drain, and gate; a floating capacitor **226** having a floating gate **218** and a control gate **230**, said floating gate being connected to said gate of said n-channel transistor; and circuitry **222** for detecting the state, whether erased or programmed, of the cell **Note: The charge**

Art Unit: 2827

state (i.e. erased or programmed) of the cell is detected by PMOS transistor 222 (see column 4, lines 50-52), wherein said circuitry for detecting the state of the cell comprises a p-channel transistor **222** having a source, a drain, and a gate, said p-channel transistor being complementary to said n-channel transistor and said gate of said p-channel transistor being connected to said floating gate. However, Killat fails to disclose: wherein an n-well diffusion region of said p-channel transistor is the control gate of said floating capacitor. The Applicant's admitted prior art teaches the control gate of the cell being a n-well diffusion region. **Page 3, lines 13-15** of Applicant's admitted prior art disclose: wherein an n-well diffusion region of said p-channel transistor is the control gate of said floating capacitor. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the control gate of the floating capacitor in the n-well diffusion region of the p-channel transistor, since Applicant discloses at **page 3, lines 13-15** that such a modification is inherently available in any process **(also see explanation above in paragraph 3)**.

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killat and Applicant's admitted prior art as applied to claim 4 above, and further in view of the US patent to Lin et al. (5,615,150), hereafter "Lin".

Pertaining to claim 9, the combined teachings of Killat and Applicant's admitted art disclose all of the claim limitations except: wherein the floating gate and the gates of the first and second transistors are embodied as a single polymer layer. Lin teaches the gates of a capacitor, PMOS transistor, and NMOS transistor being formed all in the

Art Unit: 2827

same layer. **FIG. 3** of Lin discloses: wherein the floating gate and the gates of the first and second transistors are embodied as a single polymer layer **Note: See FIG. 3 where transistor 402 (PMOS), transistor 403 (NMOS), and capacitor 430 all share a common floating gate in a single layer (also see column 3, lines 45-67).** It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the gates of the capacitor, PMOS transistor, and NMOS transistor in a single layer since such a modification would reduce the amount of patterning steps required to form the device, thus leading to a more simple process.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

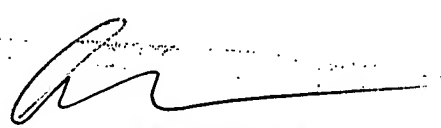
Art Unit: 2827

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kretelia Graham whose telephone number is (571) 272-5055. The examiner can normally be reached on Mon-Fri 8am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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